REMARKS

Claims 1-10 are pending in the present application. Claims 1-3 have been amended. Claims 4-10 have been presented herewith.

Priority Under 35 U.S.C. 119

Applicants note the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119, and receipt of the certified copy of the priority document.

Information Disclosure Statement

Enclosed are copies of an Information Disclosure Statement and PTO-1449 form filed on November 25, 2003, in connection with the present application. Also enclosed is a copy of a dated, stamped postcard receipt provided as evidence that the Information Disclosure Statement was received by the U.S. Patent Office. **The Examiner is respectfully requested to acknowledge receipt of the Information Disclosure Statement, and to confirm that the corresponding documents have been considered and will be cited of record in the present application**.

Specification

The title has been amended as "LSI DEVICE HAVING CORE AND INTERFACE REGIONS WITH SOI LAYERS OF DIFFERENT THICKNESS", to be more clearly indicative of the invention to which the claims are directed, as requested by the

Examiner. The Examiner is respectfully requested to approve the amended title, or in the alternative to suggest a more appropriate title.

Drawings

The drawings have been objected to under 37 C.F.R. 1.83(a), as allegedly failing to show every feature of the invention specified in the claims. The Examiner has alleged that a plurality of first MOSFETs and a plurality of second MOSFETs must be shown, or these features canceled from the claims. This objection is respectfully traversed for the following reasons.

As described beginning on page 7, line 4 of the present application with respect to Fig. 1K, in a usual MOSFET forming process, a plurality of MOSFETs 20 are formed, although only a single MOSFET 20 is shown in Fig. 1K. Also, a plurality of MOSFETs 30 are formed, although only a single MOSFET 30 is shown in Fig. 1K. Applicants respectfully submit that in view of the above description as provided in the original application, the figures should be understood to include a plurality of MOSFETs 20 and a plurality of MOSFETs 30. In order to simplify the drawings, only a single MOSFET 20 and a single MOSFET 30 are illustrated. Accordingly, Applicants respectfully submit that the drawings are in compliance with 37 C.F.R. 1.83(a), and thus respectfully urge the Examiner to withdraw this rejection for at least these reasons.

With further respect to the drawings, enclosed is one (1) red-inked drawing Annotated Sheet, wherein depleted Si channel 25 is denoted, as described on page 7,

lines 14-18 of the application. Also enclosed is one (1) drawing Replacement Sheet incorporating the drawing correction. **The Examiner is respectfully requested to acknowledge receipt and acceptance of the drawing Replacement Sheet**.

Claim Rejections-35 U.S.C. 102

Claims 1 and 3 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Numata et al. reference (U.S. Patent No. 6,043,536). This rejection is respectfully traversed for the following reasons.

The LSI device of claim 1 includes in combination an SOI substrate "having an SOI layer including a core region to which a first driving voltage is applied and an interface region to which a second driving voltage higher than the first driving voltage is applied"; a device separation region "for separating the SOI layer into the core region and the interface region, wherein a thickness of the SOI layer of the core region is thinner than a thickness of the SOI layer of the interface region"; a plurality of first MOSFETs; and a plurality of second MOSFETs. Applicants respectfully submit that the Numata et al. reference as relied upon by the Examiner does not disclose these features.

The Examiner has relied primarily upon Fig. 35 of the Numata et al. reference as described in column 21 thereof. However, the semiconductor device in Fig. 35 of the Numata et al. reference is not described or even remotely suggested as including a core region and an interface region. As described beginning in column 21, line 25 of

the Numata et al. reference, the semiconductor device of claim 35 merely includes two or more fully depleted transistors formed on a common substrate.

The Examiner has characterized Fig. 35 of the Numata et al. reference as including a core region (CR) and and interface region (IR), and has provided a copy of Fig. 35 of the Numata et al. reference as an attachment to the current Office Action dated December 22, 2004, wherein "IR" and "CR" have been drawn into the figure by the Examiner. However, as emphasized above, the Numata et al. reference as relied upon by the Examiner does not disclose or even remotely suggest that the device of Fig. 35 includes a core region and an interface region. In absence of such a specific disclosure in the Numata et al. reference, the Examiner's assertion that the Numata et al. reference discloses these features is clearly improper. Applicants therefore respectfully submit that the LSI device of claim 1 distinguishes over the Numata et al. reference as relied upon by the Examiner, and that this rejection of claims 1 and 3 is improper for at least these reasons.

With further regard to claim 1, the Numata et al. reference also fails to disclose a plurality of first MOSFETs in a core region having a first driving voltage applied thereto and a plurality of second MOSFETs in an interface region having a second driving voltage applied thereto, wherein the second driving voltage is higher than the first driving voltage.

The Examiner has asserted that it is "inherent that Numata et al. discloses a second driving voltage of an interface region is higher than the first driving voltage of a

core region because the structure of Numata et al. is formed the same as that of applicant, thus the structure of Numata et al. has the same functions as the structure of applicant".

Applicants respectfully submit that the Examiner's above noted assertion regarding the inherency of the disclosure of the Numata et al. reference is clearly improper. The Numata et al. reference does not specifically disclose core and interface regions, does not disclose respective first and second driving voltages for core and interface regions, and does not disclose a second driving voltage greater than a first driving voltage. Consequently, the structure in Fig. 35 of the Numata et al. reference is not formed the same as and does not function the same as the LSI device of claim 1, contrary to the position as asserted by the Examiner. Applicants therefore respectfully submit that the LSI device of claim 1 distinguishes over the Numata et al. reference as relied upon by the Examiner, and that this rejection of claims 1 and 3 is improper for at least these additional reasons.

Allowable Subject Matter

Applicants respectfully note the Examiner's acknowledgment that claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. However, Applicants respectfully submit that claim 2 should be considered allowable at least by virtue of dependency upon claim 1, and that amendment of claim 2 to be in independent form is thus unnecessary.

Claims 4-10

Applicants respectfully submit that claims 4 and 5 should be considered allowable at least by virtue of dependency upon claim 1.

The LSI device of claim 6 includes in combination an SOI substrate "having an SOI layer including a high speed computing region to which a first driving voltage is applied and an interface region to which a second driving voltage higher than the first driving voltage is applied"; a device separation region "for separating the SOI layer into the high speed computing region and the interface region, wherein a thickness of the SOI layer in the high speed computing region is thinner than a thickness of the SOI layer in the interface region"; a plurality of first MOSFETs; and a plurality of second MOSFETs.

Applicants respectfully submit that the prior art as relied upon by the Examiner does not disclose an LSI device including an SOI substrate having a high speed computing region and an interface region, does not disclose respective first and second driving voltages for a high speed computing region and an interface region, and does not disclose a second driving voltage that is higher than a first driving voltage. Applicants therefore respectfully submit that claims 6-10 distinguish over and would not have been obvious in view of the prior art as relied upon by the Examiner for at least these reasons.

Conclusion

Applicants respectfully submit that claims 1-3 have been amended merely to improve form, rather than to further distinguish over the relied upon prior art. As noted above, claims 1-3 distinguish over the relied upon prior art for the given reasons. Accordingly, the amendments to claims 1-3 should not be construed as narrowing scope within the meaning of *Festo*.

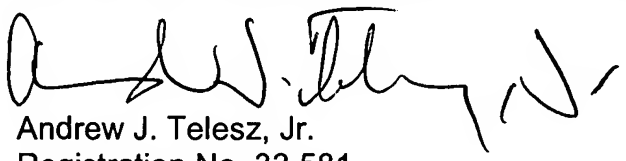
The Examiner is respectfully requested to reconsider and withdraw the corresponding rejection, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



Andrew J. Telesz, Jr.
Registration No. 33,581

One Freedom Square
11951 Freedom Drive, Suite 1260
Reston, Virginia 20190
Telephone No.: (571) 283-0720
Facsimile No.: (571) 283-0740

Enclosures: Information Disclosure Statement and 1449 Form
Copy of dated, stamped postcard receipt
One (1) drawing Annotated Sheet
One (1) drawing Replacement Sheet

FIG. 1I

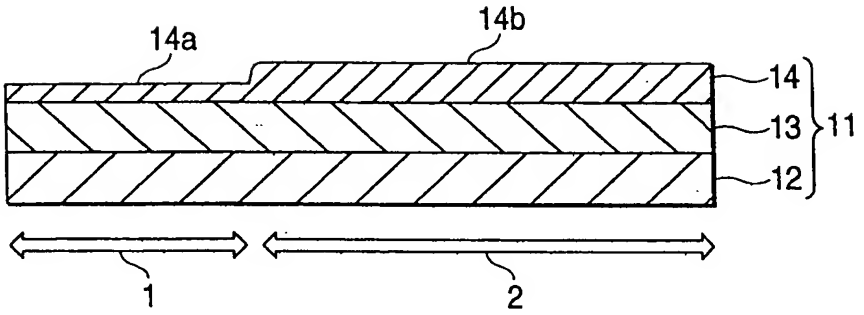


FIG. 1J

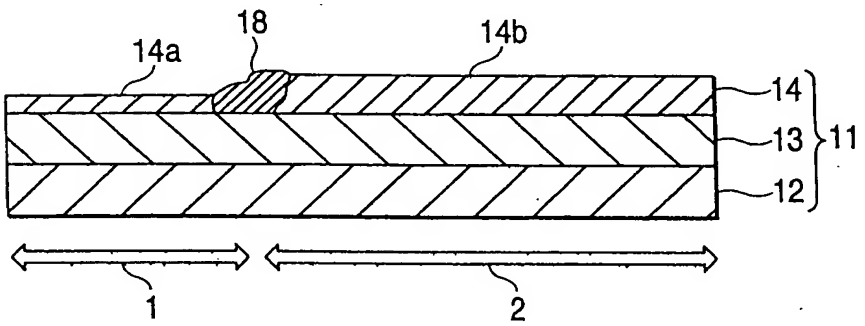


FIG. 1K